WHAT IS CLAIMED IS:

1. A design verification method for microprocessors, comprising the steps of:

generating verification programs by a computer based on a pipeline specification of a microprocessor as a target in design described in a description language readable and analyzable by a computer;

executing a simulation of a RTL description of the microprocessor based on the generated verification programs and the RTL description;

generating a pipeline simulator by the computer based on the pipeline specification;

executing a pipeline simulation based on the verification programs and the generated pipeline simulator; and

comparing a result of the simulation of the RTL description and a result of the pipeline simulation, and verifying pipeline operation of the microprocessor based on a comparison result.

2. The design verification method for microprocessors as claimed in claim 1, wherein, in the step of generating the pipeline simulator, a source program of the pipeline simulator generated by the computer based on the pipeline specification and a source program of a simulator independent of the pipeline specification are input, and the pipeline simulator is generated based on both the source programs.

3. The design verification method for microprocessors as claimed in claim 1, wherein, in the step of comparing the simulation results, it is verified that the RTL description is correct when both the result of the simulation of the RTL description and the result of the pipeline simulation are agreed.

4. The design verification method for microprocessors as claimed in claim 2, wherein, in the step of comparing the

simulation results, it is verified that the RTL description is correct when both the result of the simulation of the RTL description and the result of the pipeline simulation are agreed.

5. The design verification method for microprocessors as claimed in claim 1, wherein, the pipeline specification described in functions of C++ language is used.

6. The design verification method for microprocessors as claimed in claim 2, wherein, the pipeline specification described in functions of C++ language is used.

7. A design verification device for microprocessors, comprising:

an input section for inputting a pipeline specification of a microprocessor as a target in design described in a description language readable and analyzable by a computer;

a simulator generation section for generating a pipeline simulator by the computer based on the pipeline specification input through the input section;

a program generation section for generating verification programs by the computer based on the pipeline specification input through the input section;

a RTL simulation execution section for executing a pipeline simulation of a RTL description based on the verification programs generated by the program generation section and the RTL description of the microprocessor;

a pipeline simulation execution section for executing a pipeline simulation based on the verification programs generated by the program generation section and the pipeline simulator generated by the simulator generation section; and

a comparison section for comparing a result of the simulation executed by the RTL simulation execution section and a result of the pipeline simulation executed by the pipeline simulation execution section, and verifying an operation of the

pipeline of the microprocessor based on a comparison result.

8. The design verification device for microprocessors as claimed in claim 7, wherein the input section inputs a source program of the pipeline simulator generated by the computer based on the pipeline specification and a source program of a simulator independent of the pipeline specification, and

the simulator generation section generates the pipeline simulator based on both the source programs.

9. The design verification device for microprocessors as claimed in claim 7, wherein the comparison section verifies that the RTL description is correct when both the result of the simulation of the RTL description and the result of the pipeline simulation are agreed.

10. The design verification device for microprocessors as claimed in claim 8, wherein the comparison section verifies that the RTL description is correct when both the result of the simulation of the RTL description and the result of the pipeline simulation are agreed.

11. The design verification device for microprocessors as claimed in claim 7, wherein, the input section inputs the pipeline specification described in functions of C++ language.

12. The design verification device for microprocessors as claimed in claim 8, wherein, the input section inputs the pipeline specification described in functions of C++ language.

13. A pipeline simulator generation device comprising:

an input section for inputting a pipeline specification of a microprocessor as a target in design described in a description language readable and analyzable by a computer; and

a simulator generation section for generating a pipeline

simulator by the computer based on the pipeline specification input through the input section.

14. The pipeline simulator generation device as claimed in claim 13, wherein

the input section inputs a source program of the pipeline simulator generated by the computer based on the pipeline specification and a source program of a simulator independent of the pipeline specification, and

the simulator generation section generates the pipeline simulator based on both the source programs.

15. The pipeline simulator generation device as claimed in claim 13, wherein, the input section inputs the pipeline specification described in functions of C++ language.

16. The pipeline simulator generation device as claimed in claim 14, wherein, the input section inputs the pipeline specification described in functions of C++ language.